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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/497,916 | 02/04/2000 | Antonino Torres | S1022/8385 | 8061 |

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| EXAMINER |
|---|
| NADAV, ORI |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2811 | |

DATE MAILED: 04/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 09/497,916 | Applicant(s) TORRES ET AL. | |
|---|---|---|---|
| | Examiner ori nadav | Art Unit 2811 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *08 March 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aiello et al. (5,382,837) for reasons of record, as recited in previous office action (paper 4).

3. Claims 3-5 and 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aiello et al. (5,382,837).

Regarding claims 7 and 9, Aiello et al. teach in figures 6 and 10 an integrated circuit comprising a vertical power bipolar transistor having a terminal formed by a chip substrate of a first conductivity type 53, a control circuit thereof, the control circuit isolated from the substrate by means of an isolation region 5, 34 of a second conductivity type, and a protection structure against polarity inversion of a substrate potential comprising a first bipolar transistor T2 with an emitter connected to the isolation region (via base and collector regions) and a collector connected to a

reference potential input of the integrated circuit (via transistor T1), a bias circuit T4 for biasing the first bipolar transistor in a reverse saturated mode when the substrate potential is higher than the reference potential, and a second bipolar transistor T3 with an emitter connected to the substrate and a base coupled to the isolation region for coupling the isolation region to the substrate through a high-impedance when the substrate potential is lower than the reference potential.

Aiello et al. do not teach using the device as a protection structure against polarity inversion of a substrate potential wherein the bias circuit biases the first bipolar transistor in a reverse saturated mode when the substrate potential is higher than the reference potential.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Aiello et al.'s device as a protection structure against polarity inversion of a substrate potential in order to use the device in an application which requires a protection circuit.

Note that the recitation of using the device as a protection structure against polarity inversion of a substrate potential occurs in the preamble and a preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations

are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Furthermore, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

Regarding claim 3, Aiello et al. teach in figure 10 a first bipolar transistor is a vertical transistor having an emitter formed by the substrate, a collector formed by a second doped region of the first conductivity type, and a base formed by a first doped region of the second conductivity type formed in the substrate and within the first doped region.

Regarding claim 4, Aiello et al. teach first and third bipolar transistors are isolated from the substrate by the isolation region.

Regarding claim 5, it would be obvious for an artisan to use first conductivity type is the N type, the second conductivity type is the P type, the first and second bipolar

transistors are NPN transistors, and the third bipolar transistor is a PNP transistor in Aiello et al.'s device, because it is conventional to reverse the polarity of the transistor.

Regarding claim 8, Aiello et al. teach a second bipolar transistor forms a regulation loop that reduces parasitic transistor action from affecting the first bipolar transistor and the bias circuit.

***Response to Arguments***

4. Applicant argues on pages 5-6 that Aiello et al. do not teach a first bipolar transistor with an emitter connected to the isolation region, and a collector connected to a reference potential input of the integrated circuit.

Claims 1 and 7 recite a first bipolar transistor with an emitter connected to the isolation region, and a collector connected to a reference potential input of the integrated circuit. Claims in a pending application should be given their broadest reasonable interpretation. In re Pearson, 494F.2d 1399, 181 USPQ 641 (CCPA 1974). Therefore, the emitter can be connected to the isolation region via other elements, and the collector can be connected to the reference potential input of the integrated circuit via other elements. Aiello et al. teach a first bipolar transistor T2 with an emitter connected to the isolation region (via base and collector regions), and a collector

connected to a reference potential input of the integrated circuit (via transistor T1), as claimed. The broad recitation of the claims do not require the emitter to be directly connected to or contacting the isolation region, and the collector to be directly connected to or contacting the reference potential input of the integrated circuit.

***Conclusion***

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

**Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.**

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached at **(703) 308-2772.**

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

Ori Nadav

April 16, 2002

Steven Loke
Primary Examiner

Steven Loke